Training objectives and introduction

In this experiment the properties of an FET field effect transistor will be explored and measured on the basis of various characteristics.

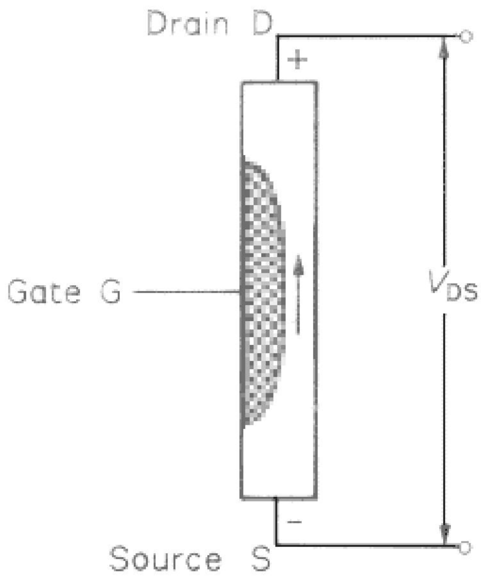
Training content

- How the field effect transistor FET operates
- How to measure the output characteristics

Introduction

The basic design of the transistor is comprised of three n- and p-doped silicon layers including two p-n junctions. In the meantime, this bipolar transistor has been replaced in many of its applications by more advanced transistor types, which feature only one p-n junction. These components are referred to as field effect transistors or FETs. As a rule, the manufacture of field effect transistors is cheaper and easier than bipolar transistors and their construction is better suited for still further minaturisation. Most transistors built into ICs and microprocessors are FETs.

N-channel FET

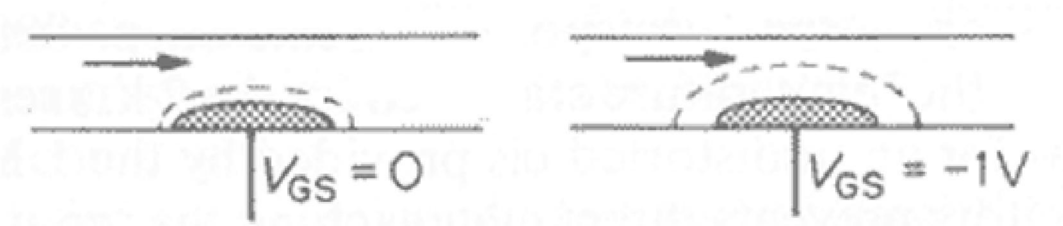


A simple field effect transistor consists of a thin block of doped silicon. In the middle of this block there is a region treated with the exact opposite type of doping material. This is done by adding suitable impurities at a single point that then spreads out into the silicon creating an electrical connection to this region. In addition to this there are two further connections set up to the two ends of the block. The connection to the middle region with opposite doping is called a **gate**, the two connections at both ends are called the **source** and **drain** . The region with

oppositely doped material comprising the gate is sized so that there is just a narrow silicon channel left behind with the original doping material. If the original silicon was n-doped, the gate is p-doped and a narrow, n-doped channel is left behind. For that reason these components are referred to as **N-channel FETs**. If, similarly p-doped material is used with an n-doped gate, this is referred to as **P-channel FETs**. N-channel FETs are used more frequently than FETs of the P-channel type. The reason for this is that their most important charge carriers are electrons which are more mobile than holes are, which assume the role of charge carrier in P-channel FETs. Consequently, FETs of the N-channel variety are usually faster than those of the P-channel type.

N-channel FETs normally feature a gate voltage that is negative with respect to the source. This means that the p-n junction in the FET *is usually reverse biased*. The transistor effect is produced by the **barrier or depletion layer**, which forms in the reverse or blocking direction at the junction. A barrier layer arises when the electrons of the material with n-doping located at the surface of the junction combine with the holes of the p-doped material. This leads to a relative lack of respective majority charge carriers on both sides of the depletion junction. The n-doped material in the proximity of the depletion zone loses electrons, the p-doped material loses holes.

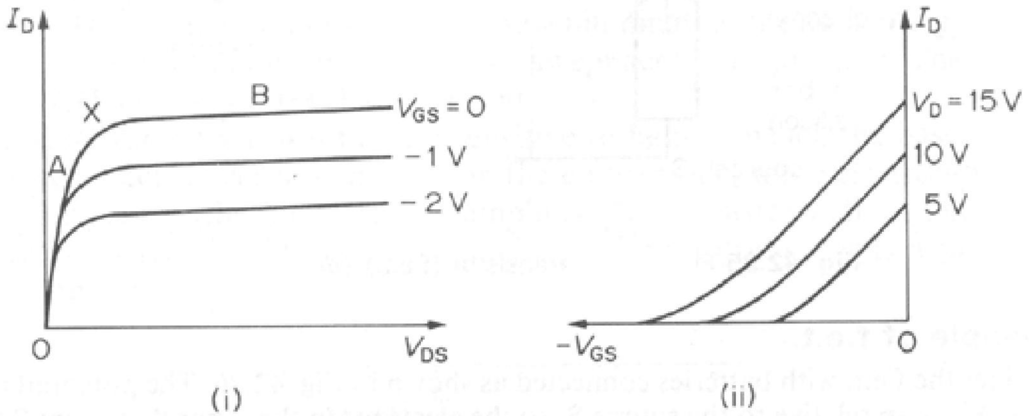
If a reverse-bias voltage is now applied across the depletion zone reversing polarity in the depletion layer, the respective minority charge carriers, i.e. the electrons in the p-doped material and the holes in the n-doped material are attracted to the junction so that even more recombinations occur near the junction and the depletion layer is widened.



A widening of the field effect transistor's depletion layer leads to a narrowing of the conducting channel. The depletion layer itself becomes less conductive because it features comparatively less charge carriers. As such the widening of the depletion layer through a negative biasing of the gate leads to a narrowing of the channel and thus to a weaker current flow between the drain and the source. Thus the depletion layer also becomes correspondingly smaller when a more positive voltage is applied to the gate. The channel becomes wider thus boosting the current flow between the drain and source. Small changes to the gate voltage can result in considerable changes in drain-source current and consequently the drain voltage itself. For that reason, field effect transistors just like bipolar transistors can be used as current and voltage amplifiers (see basic transistor circuits SO4203-7E).

As is true for bipolar transistors, there are also standard configurations for amplifier circuits with field effect transistors. The two most fundamental are the common source configuration which corresponds to the common emitter configuration of bipolar transistors and the common drain mode which in many respects resembles the common collector configuration. Both configurations are investigated in the following experiments.

The figure below shows the characteristics of the i) output voltage and ii) input voltage of a typical field effect transistor in a common source circuit.


I_D
X
B
A
V_{GS} = 0
− 1 V
− 2 V
O
V_{DS}
(i)
I_D
V_D = 15 V
10 V
5 V
$-V_{GS}$
O
(ii)